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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/351,544	07/12/99	CARNS T	ZILG.204US0

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GERALD P. PARSONS
MAJESTIC, PARSONS, SIEBERT & HSUE P.C.
FOUR EMBARCADERO CENTER, SUITE 1100
SAN FRANCISCO CA 94111-4106

EXAMINER	
BROCK II,P	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 10/04/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trad marks

Office Action Summary	Application No.	Applicant(s)	
	09/351,544	CARNS ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- Th MAILING DATE of this communication app ars on th cover sh et with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *26-30* is/are allowed.

6)☒ Claim(s) *1-3 and 8-25* is/are rejected.

7)☒ Claim(s) *4-7* is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 July 1999* is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☐ received.

2.☐ received in Application No. (Series Code / Serial Number) _____.

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15)☒ Notice of References Cited (PTO-892)
16)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17)☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4*.
18)☐ Interview Summary (PTO-413) Paper No(s). _____.
19)☐ Notice of Informal Patent Application (PTO-152)
20)☐ Other:

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a) because they fail to show units of measure for the x and y axis for figure 1 as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Correction is required.

2. Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect can be deferred until the application is allowed by the examiner.

Specification

3. The disclosure is objected to because of the following informalities:

a. On pages 7 and 14, lines 21 and 29 respectively, "form" should be replaced with the word "from".

b. Page 14, line 19, the sentence starting with the words "These last..." doesn't make any sense.

Appropriate correction to these and any other minor informality is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 13-18, 21 and 25 are rejected under 35 U.S.C. 102(a) as being anticipated by Watanabe.

In regard to claim 13, Watanabe discloses a method of forming a capacitor in an integrated circuit with a bottom electrode layer (6) over a semiconductor body (2), forming a dielectric layer (7) over a portion of the bottom electrode, and a top electrode layer (8) over a portion of the dielectric layer as shown in figure 1a. A portion of the top electrode layer is removed to expose a portion of the dielectric layer (7), and an insulating layer (10) is formed over at least a portion of the top electrode (8a), and the exposed portion of the dielectric layer (7) as shown in figures 1b and 3a. Figures 1c and 3b further disclose removing a portion of the insulating layer and a portion of the dielectric layer, thereby exposing at least a portion of the lower electrode layer and forming side wall spacers (10a), wherein the side wall spacers are formed on the side walls of the top electrode (8a) and of the inter-electrode region of the dielectric (7a).

In regard to claims 14, 15, and 21, a non-insulating layer (20) is formed over at least a portion of the resultant structure after removing a portion of the insulating layer and a portion of the dielectric layer as illustrated in figure 3c of Watanabe. The non-insulating layer (20) is an anti-reflection film. It is inherent to believe that an anti-reflection film is an anti-reflective layer or an anti-reflective coating.

In regard to claims 16-18, it is inherent to believe that the insulating layer (7) of Watanabe can be formed by deposition or by being grown. It is inherent that an anneal is performed after an insulating layer is formed by deposition.

In regard to claim 25, Watanabe discloses the bottom electrode layer additionally being used to form the gate of one or more transistors on the integrated circuit in figures 3c and 3d.

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

6. Claims 1-3, 8, and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Nishihori et al.

In regards to claim 1, Nishihori et al. discloses a method for forming a capacitor in an integrated circuit, in figure 11a, by first forming a bottom electrode layer (32) on a semiconductor body (31). A dielectric layer (34) is formed over at least a portion of the bottom electrode layer (32), and a top electrode layer (35) is formed over at least a portion of the dielectric layer as shown in figure 11b. A portion of the top electrode layer (35) is removed to expose a portion of the dielectric layer (34) while subsequently removing at least a portion of the exposed portion of the dielectric layer to expose a portion of the bottom electrode layer (32) as disclosed in figure 11c. Figure 11c also shows forming a conformal insulating layer (36) over at least a portion of the exposed portion of the bottom electrode layer (32) proximate to the exposed dielectric layer (34), the exposed dielectric layer and at least a part of the top electrode layer (35a) proximate to the exposed dielectric layer.

In regard to claim 2, Nishihori et al. also discloses in figure 11c forming a non-insulating layer (37) over at least a portion of the resultant structure after forming the conformal insulating layer (36).

In regard to claims 3 and 8, Nishihori et al. uses examples of a non-insulating layer of Au (columns 8 and 9, lines 2 and 47 respectively). By virtue of Au being a metal one of its physical properties inherently would classify it as an anti-reflective layer or an anti-reflective coating.

In regard to claim 12, Nishihori et al. discloses in figures 11a and 11b that the bottom electrode layer is additionally used to form the gate (33) of one or more transistors formed on the integrated circuit.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishihori et al.

In regard to claim 10, Nishihori et al. does not disclose a method for depositing the anti-reflective layer as applied to claims 1-3 above. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a plasma enhanced chemical vapor deposition anti-reflective layer in order to deposit the anti-reflective layer.

In regard to claim 9, Nishihori et al. does not disclose the use of titanium nitride as the anti-reflective layer as applied to claims 1-3 above. Nishihori et al. does disclose the use of titanium nitride as the top and bottom electrodes (column 7, lines 31-36). Because the top and

bottom electrodes must be conductive and the anti-reflective layer is conductive, it would have been obvious to one of ordinary skill in the art at the time of the present invention to use the titanium nitride as the anti-reflective layer.

9. Claims 19, 20 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe as applied to claims 13-15 above.

Watanabe discloses the use of an oxide layer with a thickness of 2500 angstroms as the insulating layer in column 8, lines 42-45. Watanabe does not teach an oxide layer of thickness 500-2000 angstroms. With regard to claim 19, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the 2500 angstrom thick oxide layer of Watanabe to achieve the claimed thickness of 2000 angstroms since such changes in dimensions need no undue experimentation.

With regard to claim 20, the spacer width is determined by the thickness of the oxide layer. It would have been obvious to one of ordinary skill in the art at the time of the invention to have a side wall spacer thickness in the range of 500 to 2000 angstroms which is equal to the thickness of the oxide layer of claim 19 above.

Watanabe does not disclose a method for depositing the anti-reflective layer. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the conventional plasma enhanced chemical vapor deposition ~~anti-reflective layer~~ method in order to deposit the anti-reflective layer.

10. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nishihori et al. as applied to claims 1-3 and 10 above, and further in view of Randazzo.

Nishihori et al. does not disclose the use of the plasma enhanced chemical vapor deposition anti-reflective layer having a thickness in the range from 300 to 400 angstroms. Randazzo teaches in column 4, lines 45-47 an anti-reflective layer having a thickness in the range of 300 to 400 angstroms. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use plasma enhanced chemical vapor deposition of Randazzo for depositing the anti-reflective layer of Nishihori in order to have the thickness of the conductor in a desirable range.

11. Claims 22 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe as applied to claims 13-15 and 23 above, and further in view of Randazzo.

In regard to claims 22 and 24, Watanabe does not disclose the thickness of the antireflective layer or the use of titanium nitride as an anti-reflective layer. Randazzo teaches the use of an anti-reflective layer of titanium nitride with a thickness in the range of 300-400 angstroms (column 4, lines 45-47). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the 300-400 angstrom thick, titanium nitride, anti-reflective layer of Randazzo as the anti-reflective layer of Watanabe in order to form a barrier layer between the top electrode and a metal contact.

Allowable Subject Matter

12. Claims 4-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. Claims 26-30 are allowed.

14. The following is an examiner's statement of reasons for allowance:

Nishihori et al. teaches the use of a conformal insulating layer as applied to claims 1-3 above. Nishihori et al. does not teach the use of a conformal insulating layer 20-70 angstroms thick, as applied to claim 4.

Watanabe discloses the use of forming a bottom electrode layer on a semiconductor device, forming a dielectric layer over at least a portion of the bottom electrode layer, forming a top electrode layer over at least a portion of the dielectric layer, and removing a portion of the top electrode layer to expose at least a portion of the dielectric layer. Watanabe does not disclose forming an anti-reflective layer over at least a portion of the top electrode and the exposed portion of the dielectric layer as applied to claim 23.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yoshio et al., Toshiyuki et al., Masao, Chauang, Huang, Natsume, Kwon et al., Takahashi et al., and Meinick et al. discuss capacitors with some form of spacer or insulating layer. Kim et al. discusses the us of anti-reflective coatings.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mashid Saadat can be reached on (703)308-4915. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

PEBK

Paul E Brock II
October 2, 2000

Mahshid Saadat

Mahshid Saadat
Supervisory Patent Examiner
Technology Center 2800